IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s):	Azadet et al.
Case:	13-5
Serial No.:	09/834,668
Patent No.:	7,000,175
Issue Date:	February 14, 2006
Group:	2133
Examiner:	Joseph D. Torres

Title: Method and Apparatus for Pipelined Joint Equalization and Decoding for Gigabit Communications

---

REQUEST FOR CERTIFICATE OF CORRECTION OF
PATENT FOR PTO MISTAKE(S) UNDER 37 C.F.R. 1.322(a)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. §1.322, the patentee for the above-identified patent hereby requests the issuance of a Certificate of Correction with respect to errors in the above-identified patent.

The errors are set forth on the proposed Certificate of Correction (PTO-1050) submitted herewith, in duplicate.

There is no additional fee due in conjunction with this Certificate of Correction. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 50-0762** as required to correct the error.

Respectfully,

Date: February 25, 2010

Kevin M. Mason
Attorney for Applicant(s)
Reg. No. 36,597
Ryan, Mason & Lewis, LLP
1300 Post Road, Suite 205
Fairfield, CT 06824
(203) 255-6560

PTO/SB/44 (02-01)
Approved for use through 01/31/2004. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 7,000,175
DATED : February 14, 2006
INVENTOR(S) : Azadet et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the specification, column 8, line 31, before "need not" replace "$\hat{a}_{n-K-1}(\rho_{n-1})$)" with --$\hat{a}_{n-K-1}(\rho'_{n-1})$)--.

Column 8, line 33, after "state" replace "ρ_{n-1}" with --ρ'_{n-1}--.

Column 8, line 35, after "state" replace "ρ_{n-1}" with --ρ'_{n-1}--.

Column 8, line 52, before "is" and after "where" replace "$\Lambda_n(z_n, a_n, \rho'_n)$" with -- $\Lambda_n(z_n, a_n, \rho'_n)$ --.

Column 9, line 21, after "symbols" replace "$(\hat{a}_{n-M-1}\rho'_{n-M})$," with --$(\hat{a}_{n-M-1}(\rho'_{n-M})$,--.

Column 9, line 22, before "are identical" replace "$\hat{a}_{n-M-K}\rho'_{n-M})$)" with --$(\hat{a}_{n-M-K}(\rho'_{n-M}))$--.

Column 9, line 24, before "is fixed" replace "$v_n\rho'_{n-M}$)" with -- $v_n(\rho'_{n-M})$--.

Column 14, line 3, after "coefficients" replace "$\{f^{3,j}$" with -- $\{f_{3,j}$ --.

Column 15, line 7, replace "$f1\tilde{a}_{n,j}$" with --$f_i\tilde{a}_{n,j}$ --.

Column 15, line 28, after "symbol" and before "is selected" replace "a_{n+1}" with -- $a_{n+1,j}$ --.

MAILING ADDRESS OF SENDER:
Ryan, Mason & Lewis, LLP
1300 Post Road - Suite 205
Fairfield, Connecticut 06824

PATENT NO. 7,000,175

No. of additional copies

PTO/SB/44 (02-01)
Approved for use through 01/31/2004. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 7,000,175
DATED : February 14, 2006
INVENTOR(S) : Azadet et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the specification, column 15, beginning on line 66, the following heading and paragraph should be re-inserted:

-- Survivor Memory Unit

The merge depth of the exemplary 1000BASE-T trellis code is 14. The SMU must be implemented using the register-exchange architecture described in R. Cypher and C.B. Shung, "Generalized Trace-Back Techniques for Survivor Memory Management in the Viterbi Algorithm," J. VLSI Signal Processing, Vol. 5, 85-94 (1993), as the survivor symbols corresponding to the time steps $n-12, n-11, \ldots, n$ are needed in the DFU without delay and the latency budget specified in the 1000BASE-T standard is very tight. The proposed register-exchange architecture with merge depth 14 is shown in FIG. 18, where only the first row storing the survivor sequence corresponding to state zero is shown. $\underline{SX}_n(\rho_n)$ denotes the 4D symbol decision corresponding to 4D subset SX and a transition from state ρ_n. The multiplexers in the first column select the 4D survivor symbols $\{\underline{\hat{a}}_n(\rho_{n+1})\}$, which are part of the survivor path into $\{\rho_{n+1}\}$. These 4D survivor symbols are required in the ISI-MUXU 1416 and 1D-BM-MUXU 1428 to select the appropriate partial ISI estimates and 1D branch metrics, respectively. The survivor symbols $\{\underline{\hat{a}}_{n-1}(\rho_n), \underline{\hat{a}}_{n-2}(\rho_n), \ldots, \underline{\hat{a}}_{n-12}(\rho_n)\}$ which are stored in the registers corresponding to the first, second, ... 12th column are used in the LA-DFU 1412 to compute the partial ISI estimates $v_{n+2,j}(\rho_n)$. --

In claim 3, column 16, line 36, before "from" replace "decisions" with -- decision --.

MAILING ADDRESS OF SENDER:
Ryan, Mason & Lewis, LLP
1300 Post Road - Suite 205
Fairfield, Connecticut 06824

PATENT NO. 7,000,175

No. of additional copies